T-46-13-29

Am27C128

16,384 x 8-Bit CMOS EPROM

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- Fast access time — 55 ns
- Low power consumption:
  - 100 μA maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved pinout
- ±10% power supply tolerance available
- One-Time Programmable (OTP) Flashrite™ programming
- Latch-up protected to 100 mA from −1 V to V_{CC} +1 V

GENERAL DESCRIPTION

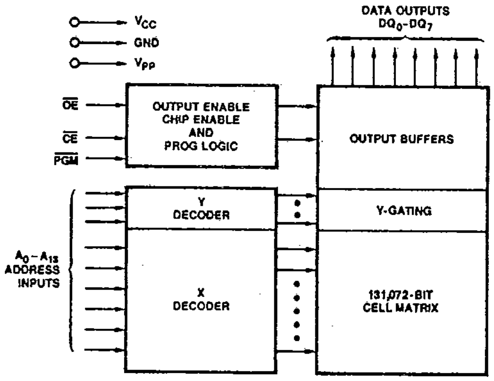
The Am27C128 is a 128K-bit, ultraviolet erasable programmable read-only memory. It is organized as 16,384 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C128 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 μW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C128 supports AMD's interactive programming algorithm (1-ms pulses) resulting in typical programming times of less than two minutes.

BLOCK DIAGRAM



BD008360

PRODUCT SELECTOR GUIDE

Family Part No.	Am27C128							
Ordering Part No: ±5% V_{CC} Tolerance	−55	−75	−95	−125	−155	−205	−255	−305
±10% V_{CC} Tolerance	−	−70	−90	−120	−150	−200	−250	−300
Max. Access Time (ns)	55	70	90	120	150	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	40	50	65	75	100	120

Flashrite is a trademark of Advanced Micro Devices Inc.

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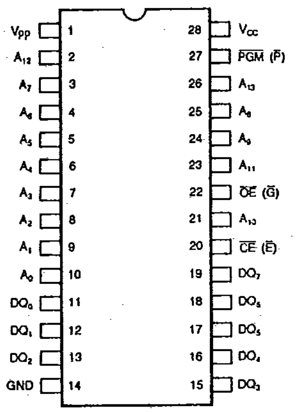
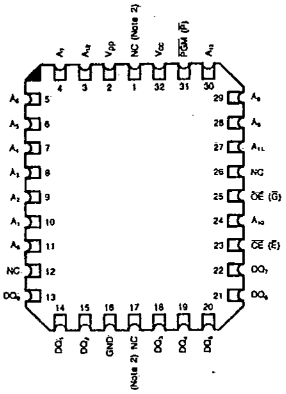
CONNECTION DIAGRAMS
Top View

DIP



CD011810

LCC*

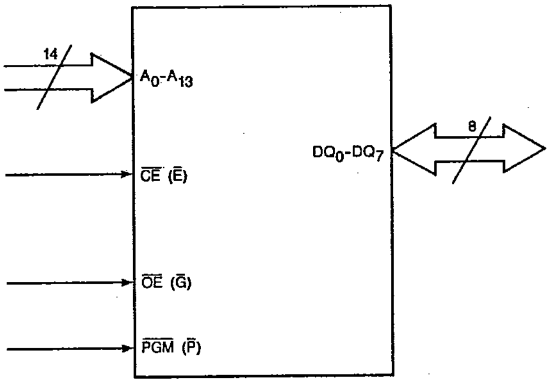


CD011820

Notes: 1. JEDEC nomenclature is in parentheses
2. Don't use (DU) for PLCC.

* Also available in 32-pin rectangular plastic leaded chip carrier.

LOGIC SYMBOL



LS003360

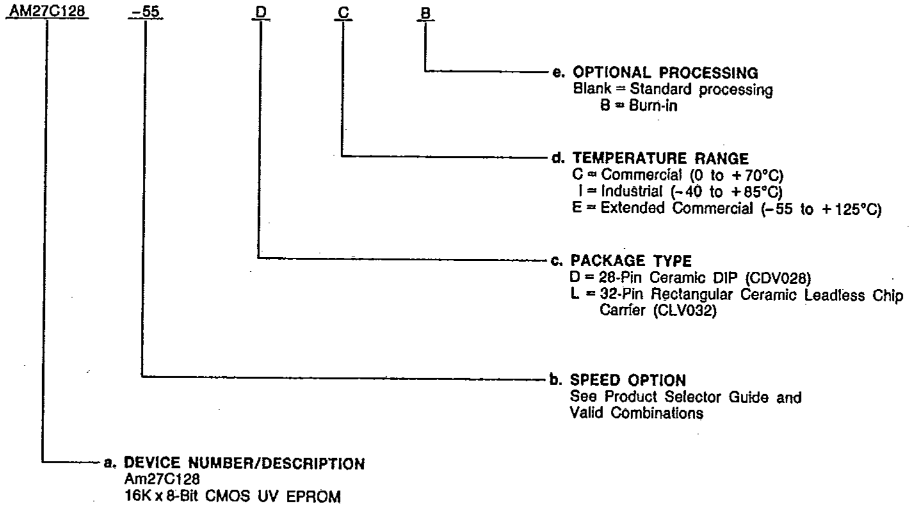
PIN DESCRIPTION

A_0 - A_{13} = Address Inputs
$\overline{CE}$ ($\overline{E}$) = Chip Enable Input
DQ_0 - DQ_7 = Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$) = Output Enable Input
$\overline{PGM}$ ($\overline{P}$) = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Supply Voltage
GND = Ground
NC = No Internal Connection
DU = No External Connection

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
E = Extended Commercial (–55 to +125°C)

c. PACKAGE TYPE
D = 28-Pin Ceramic DIP (CDV028)
L = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLV032)

b. SPEED OPTION
See Product Selector Guide and Valid Combinations

a. DEVICE NUMBER/DESCRIPTION
Am27C128
16K x 8-Bit CMOS UV EPROM

Valid Combinations	
AM27C128-55	DC, DCB, LC, LCB
AM27C128-70	
AM27C128-75	
AM27C128-95	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C128-125	
AM27C128-155	
AM27C128-205	
AM27C128-255	
AM27C128-305	
AM27C128-90	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-250	
AM27C128-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing

AM27C128 -120 P C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 28-Pin Plastic DIP (PD 028)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)

b. SPEED OPTION
See Product Selector Guide and Valid Combinations

a. DEVICE NUMBER/DESCRIPTION
Am27C128
16K x 8-Bit CMOS OTP EPROM

Valid Combinations	
AM27C128-120	JC, PC
AM27C128-125	
AM27C128-150	
AM27C128-155	
AM27C128-200	
AM27C128-205	
AM27C128-250	
AM27C128-255	
AM27C128-300	
AM27C128-305	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish

AM27C128 -90 /B X A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
X = 28-Pin Ceramic DIP (CDV028)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLV032)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
See Product Selector Guide and Valid Combinations

a. DEVICE NUMBER/DESCRIPTION
Am27C128
16K x 8-Bit CMOS UV EPROM

Valid Combinations	
AM27C128-90	/BXA, /BUA
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-250	
AM27C128-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C128

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C128 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C128. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The Am27C128 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C128, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C128 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C128

Upon delivery, or after each erasure, the Am27C128 has all 131,072 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C128 through the procedure of programming.

The programming mode is entered when 12.5 ±0.5 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{PGM}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart in Figure 1 shows AMD's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C128. This part of the algorithm is done at $V_{CC} = 6.0$ V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = 5$ V ± 5%.

Flashrite

The OTP EPROM Flashrite programming algorithm (shown in Figure 2) reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTP EPROM.

The Flashrite programming algorithm programs and verifies at $V_{CC} = 6.25$ V and $V_{PP} = 12.75$ V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP} = 5.25$ V.

Program Inhibit

Programming of multiple Am27C128s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C128 may be common. A TTL low-level program pulse applied to an Am27C128 $\overline{PGM}$ input with $V_{PP} = 12.5 \pm 0.5$ V and $\overline{CE}$ LOW will program that Am27C128. A high-level $\overline{CE}$ input inhibits the other Am27C128s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.0 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C128.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C128. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$), the device identifier code. For the Am27C128, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C128 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 μA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27C128 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	V_{CC}	High Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (CMOS)		V_{CC} ± 0.3 V	X	X	X	X	V_{CC}	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Notes 3 & 4)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	16H

Notes: 1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0$ V ± 0.5 V
3. $A_1 - A_8 = A_{10} - A_{12} = V_{IL}$
4. $A_{13} = X$
5. See DC Programming characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
OTP Products .... -65 to $+125°C$
All Other Products .... -65 to $+150°C$
Ambient Temperature
with Power Applied .... -55 to $+125°C$
Voltage with Respect to Ground:
All pins except A_9, V_{PP}, and
V_{CC} .... -0.6 to V_{CC} $+0.5$ V
A_9 and V_{PP} .... -0.6 to 13.5 V
V_{CC} .... -0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Minimum DC voltage on input or I/O is -0.5 V. During transitions, the inputs may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O is V_{CC} $+0.5$ V which may overshoot to V_{CC} $+2.0$ V for periods up to 20 ns.

2. For A_9 and V_{PP} the minimum DC input is -0.5 V. During transitions, A_9 and V_{PP} may undershoot GND to -2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0 to $+70°C$
Industrial (I) Devices
Case Temperature (T_C) .... -40 to $+85°C$
Extended Commercial (E) Devices
Case Temperature (T_C) .... -55 to $+125°C$
Military (M) Devices
Case Temperature (T_C) .... -55 to $+125°C$
Supply Read Voltage:
V_{CC}/V_{PP} for Am27C128-XX5 ....$+4.75$ to $+5.25$ V
V_{CC}/V_{PP} for Am27C128-XX0 ....$+4.50$ to $+5.50$ V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400$ µA		2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage			-0.3	$+0.8$	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		50	
I_{CC2}	V_{CC} Standby Current (Note 9)	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$			100	µA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400$ µA		2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{IH}	Input HIGH Voltage			$V_{CC}-0.3$	$V_{CC}+0.3$	V
V_{IL}	Input LOW Voltage			-0.3	$+0.8$	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	

DC CHARACTERISTICS over operating range unless otherwise specified (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}	C/I Devices		10	μA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)	C/I Devices		25	mA
			E/M Devices		25	
I_{CC2}	V_{CC} Standby Current (Note 9)	$\overline{CE} = V_{CC} \pm 0.3$ V	C/I Devices		100	μA
			E/M Devices		120	
I_{PP1}	V_{PP} Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$			100	μA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	$V_{IN} = 0$ V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	$V_{IN} = 0$ V	12	20	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	$V_{IN} = 0$ V	9	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$ V	8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C128 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. $T_A = 25°C$, f = 1 MHz.
8. Minimum DC input voltage is −0.5 V. During transitions, the inputs may undershoot to −2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.
9. For Am27C128-305, I_{CC1} = 50mA, I_{CC2} (TTL) = 5mA, I_{CC2} (CMOS) = 500μA, and I_{PP1} (Read) = 1mA maximum.

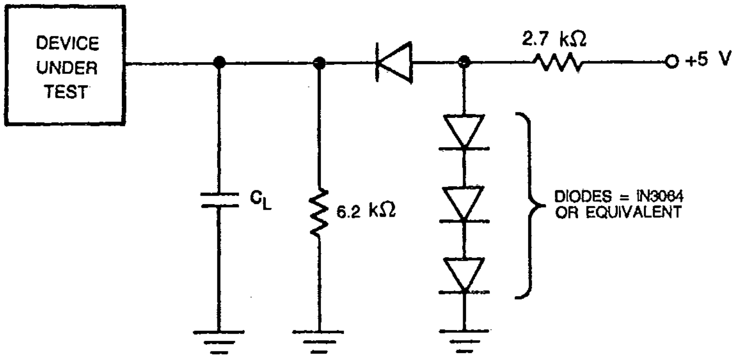
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27C128								Unit
JEDEC	Standard				– -55	-70, -75	-90, -95	-120, -125	-150, -155	-200, -205	-250, -255	-300, -305	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.									ns
				Max.	55	70	90	120	150	200	250	300	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.									ns
				Max.	55	70	90	120	150	200	250	300	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.									ns
				Max.	35	40	40	50	65	75	100	120	
t_{EHQZ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 2)		Min.									ns
				Max.	25	25	25	35	50	55	60	75	
t_{AXOX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$,whichever occurred first		Min.	0	0	0	0	0	0	0	0	ns
				Max									

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C128 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. For the −55, −70, −75:
   Output Load: 1 TTL gate and C_L = 30 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0 to 3 V,
   Timing Measurement Reference Level −1.5 V inputs and outputs.

   For all other Versions:
   Output Load: 1 TTL gate and C_L = 100 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

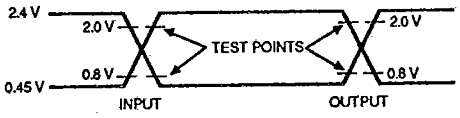
SWITCHING TEST CIRCUIT



TC003193

C_L = 100 pF including jig capacitance (30 pF for −55, −70, and −75)

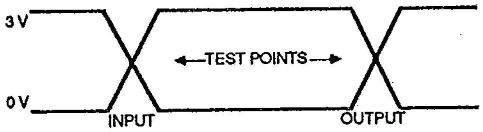
SWITCHING TEST WAVEFORMS



11420-001A

WF026820

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ⩽20 ns.



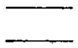
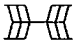
11420-002A

WF026830

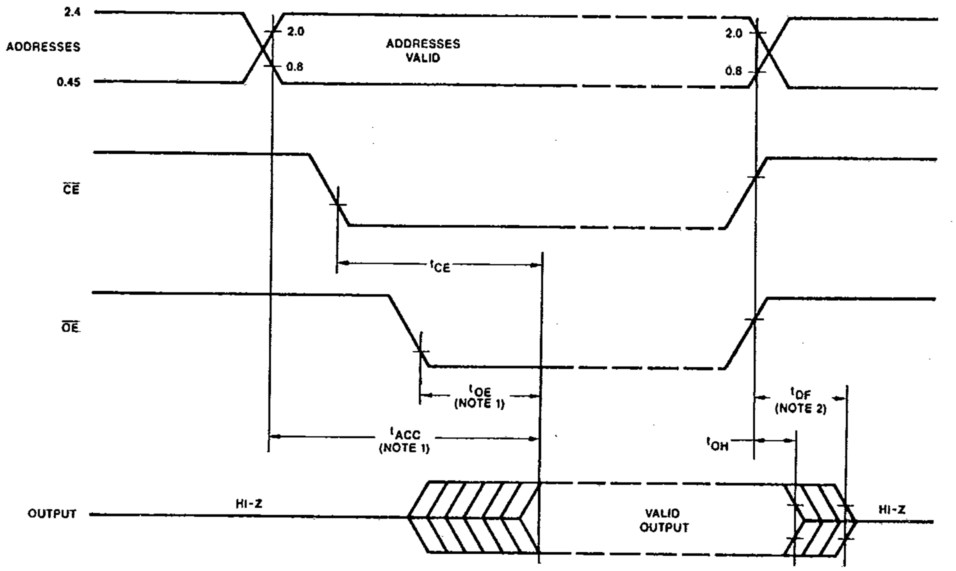
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ⩽20 ns for −55, −70, and −75 devices.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF001324

Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHARTS

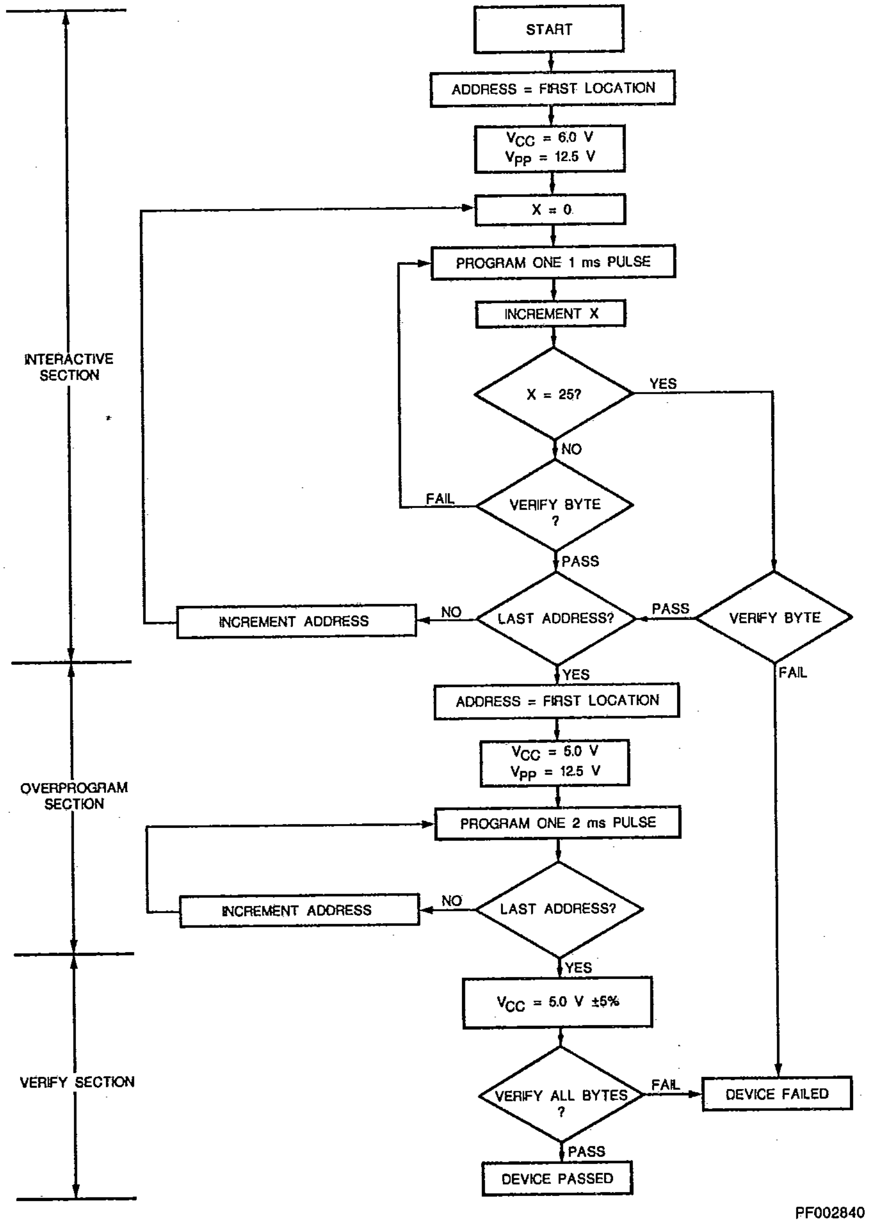
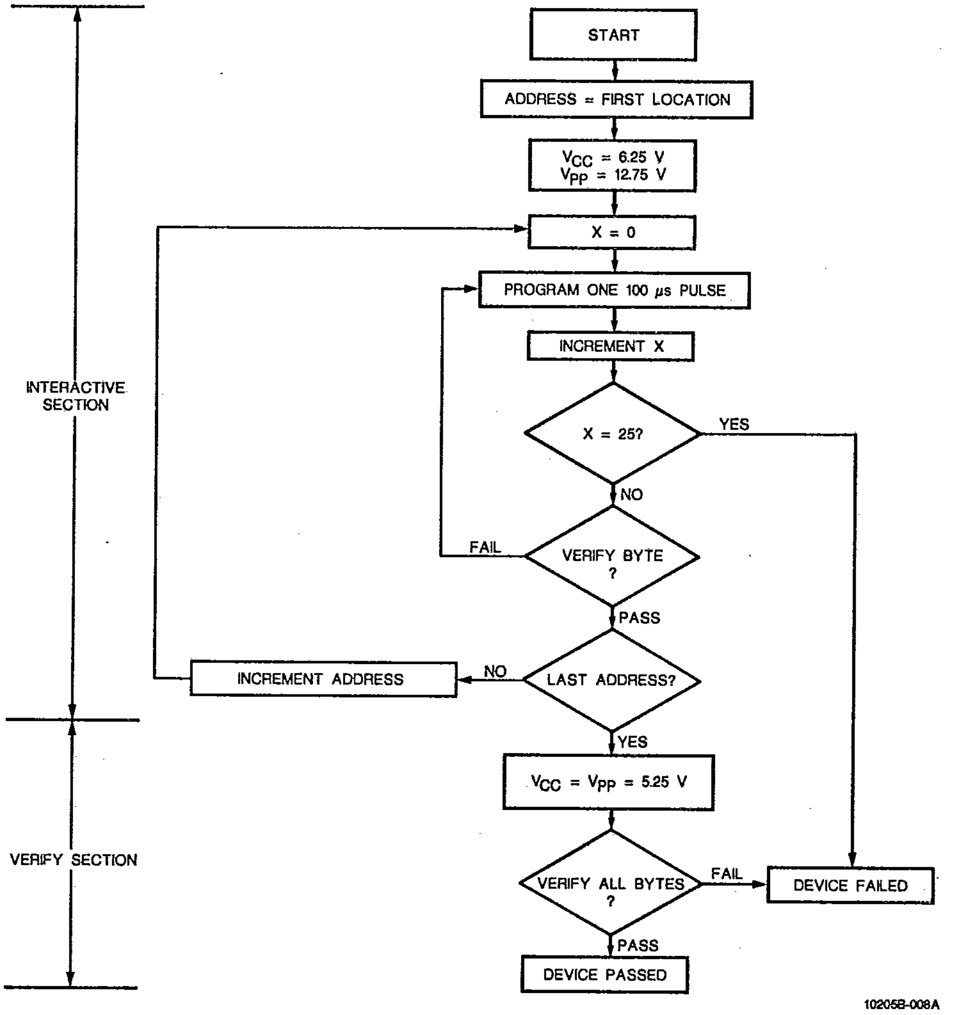


Figure 1. Interactive Programming Flow Chart

T-46-13-29



PF002490

Figure 2. Flashrite Programming Flow Chart for OTP EPROM

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3).

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	μA
V_{IL}	Input LOW Level (All Inputs)		−0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = −400 μA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC3}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC1}	Interactive Supply Voltage		5.75	6.25	V
V_{PP1}	Interactive Programming Voltage		12.0	13.0	V
V_{CC2}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP2}	Flashrite Programming Voltage		12.5	13.0	V

SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3).

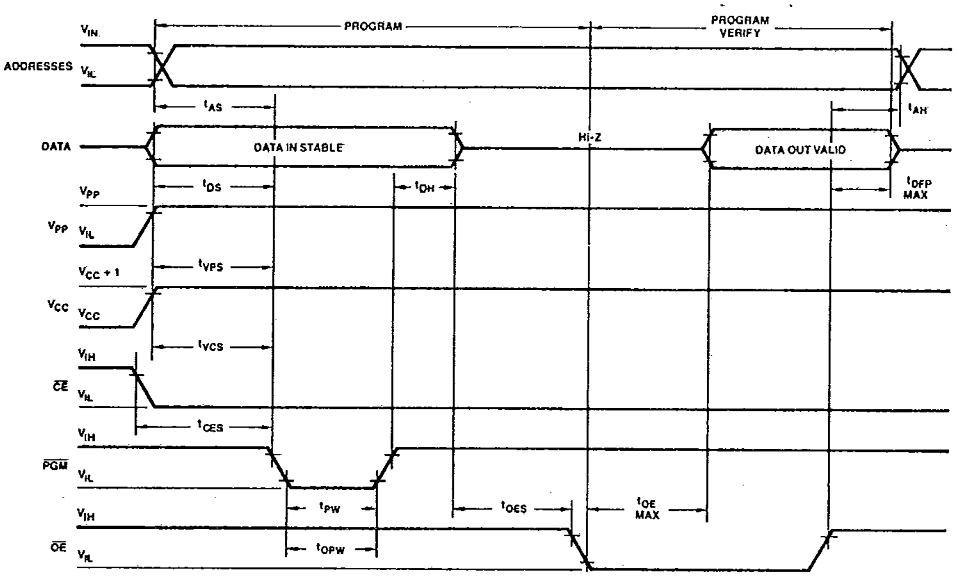
Parameter Symbols		Parameter Description		Min.	Max.	Unit
JEDEC	Standard					
t_{AVEL}	t_{AS}	Address Setup Time		2		μs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time		2		μs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time		2		μs
t_{DVEL}	t_{DS}	Data Setup Time		2		μs
t_{GHAX}	t_{AH}	Address Hold Time		0		μs
t_{EHDX}	t_{DH}	Data Hold Time		2		μs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay		0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time		2		μs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	Flashrite	95	105	μs
			Interactive	0.95	1.05	μs
t_{ELEH2}	t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width (Interactive)		1.95	2.05	ms
t_{VCS}	t_{VCS}	V_{CC} Setup Time		2		μs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$			150	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. When programming the Am27C128, a 0.1-μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.

3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



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Notes: 1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.